

**TOWNSEND**  
*and*  
**TOWNSEND**  
*and*  
**CREW**

LLP

Denver, Colorado  
Tel 303 571-4000

San Francisco

Palo Alto, California  
Tel 650 326-2400Two Embarcadero Center  
Eighth Floor  
San Francisco  
California 94111-3834  
Tel 415 576-0200  
Fax 415 576-0300Seattle, Washington  
Tel 206 467-9500Walnut Creek, California  
Tel 925 472-5000**FACSIMILE COVER SHEET**

Date: <b>June 18, 2003</b>	Client & Matter Number : <b>016301-033100us</b>	No. Pages (including this one): <b>3</b>
To: <b>Examiner Novacek USPTO</b>	At Fax Number: <b>703-746-4064</b>	Confirmation Phone Number: <b>703-308-5840</b>
<b>From : Patrick R. Jewik (4529)</b>		

**Message:**

Re: Telephonic Interview For 09/692,527 next Monday at 11:00 (EST)

Dear Examiner Novacek:

Pursuant to our phone conversation, attached are two pages from a semiconductor processing textbook. I'd like to talk about the attached article, the pending rejection(s), and possible amendments to expedite the prosecution.

Thanks for your time.

Patrick Jewik

415-273-7529

Original Will:	<input type="checkbox"/>	BE SENT BY MAIL	<input type="checkbox"/>	BE SENT BY FEDEX/OVERNIGHT COURIER	<input type="checkbox"/>	BE SENT BY MESSENGER	<input checked="" type="checkbox"/>	NOT BE SENT
----------------	--------------------------	-----------------	--------------------------	------------------------------------	--------------------------	----------------------	-------------------------------------	-------------

Faxed: Return to: Patrick R. Jewik - (4529)

If you have problems with reception please call Fax Services at extension 4659

**Important**

This message is intended only for the use of the individual or entity to which it is addressed and may contain information that is privileged, confidential, and/or exempt from disclosure by applicable law or court order. If the reader of this message is not the intended recipient, or the employee or agent responsible for delivering the message to the intended recipient, you are hereby notified that any dissemination, distribution, or copying of this communication is strictly prohibited. If you have received this communication in error, please notify us immediately by telephone and return the original message to us at the above address via the United States Postal Service. Thank you.

SF 1469605 v1

# Microchip Fabrication

**A Practical Guide to Semiconductor Processing**

**Peter Van Zant**

## Other Reference Books of Interest by McGraw-Hill

### Handbooks

- **ERICKSON • Television Engineering Handbook**
- **CHEN • Computer Engineering Handbook**
- **COOKES • Printed Circuits Handbook**
- **DI GIACOMO • Digital Bus Handbook**
- **DI GIACOMO • VLSI Handbook**
- **FUNK AND CURRINGTON • Electronics Engineers' Handbook**
- **HARPER • Electronic Packaging and Interconnection Handbook**
- **JURAN AND GRYNA • Juran's Quality Control Handbook**
- **ROBINSKICH • Digital Filter Designer's Handbook**
- **SEIDENFAND AND HARPER • Hybrid Microelectronic Handbook**
- **TOMA • Engineering Mathematics Handbook**
- **WILKINSON • Electro-Optics Handbook**
- **WILLIAMS AND TAYLOR • Electronic Filter Design Handbook**

### Other

- **ANTONETTI • Power Integrated Circuits**
- **ASTROMINETI AND MASSERETTO • Semiconductor Device Modeling with SPICE**
- **BEST • Phase-Locked Loops**
- **BUCHANAN • CMOS/TTL Digital Systems Design**
- **BUCHANAN • BiCMOS/CMOS Systems Design**
- **DYERS • Printed Circuit Board Design with Microcomputers**
- **ELLIOTT • Integrated Circuits Fabrication Technology**
- **ELLIOTT • The Laser Guidebook**
- **KOBAYASHI • Inside SPICE**
- **SHIMIZU • Thin Film Deposition**
- **VLSI Technology**
- **VARVARIS • Mixed Analog Digital VLSI Devices and Technology: An Introduction**
- **YEH • LSI/VLSI Testability Design**
- **WORCESTER • Circuit Design for Electronic Instrumentation**
- **WORR • Electro-Optical System Design**

Received from <415 576 0300> at 6/18/03 1:10:57 PM [Eastern Daylight Time]

To order or receive additional information on these or any other McGraw-Hill titles, please call 1-800-822-8768 in the United States. In other countries, contact your local McGraw-Hill representative.

KEY = WM16XXA

**McGraw-Hill**  
 New York San Francisco Washington, D.C. Auckland Bogota  
 Caracas London Madrid Mexico City Milan  
 Monterrey New Delhi San Juan Singapore  
 Sydney Tokyo Toronto

### Subsurface reflectivity

The high-intensity exposing radiation ideally is directed at a 90° angle to the wafer surface. When this ideal situation exists, exposing wave is reflected directly up and down in the resist, leaving a well-defined exposed image (Fig. 10.7). In reality, some of the exposing waves are traveling at angles other than 90° and expose unwanted portions of the resist.

This subsurface reflectivity varies with the surface layer material and the surface smoothness. Metal layers, especially aluminum and aluminum alloys, have higher reflectivity properties. A goal of the deposition processes is a consistent and smooth surface to control this form of reflection.

Reflection problems are intensified on wafers with many steps, also called a varied topography. The sidewalls of the steps reflect radiation at angles into the resist, causing poor image resolution. A particular problem is light interference at the step that causes a "notching" of the pattern as it crosses the step (Fig. 10.8).

### Antireflective Coatings

Antireflective coatings (ARCs) spun onto the wafer surface before the resist (Fig. 10.9) can aid the patterning of small images. The ARC layer brings several advantages to the masking process. First is a planarizing of the surface, which makes for a more planarized resist layer. Second, an ARC cuts down on light scattering from the surface into the resist, which helps in the definition of small images. An ARC can also minimize standing wave effects and improve the image contrast. The latter benefit comes from increased exposure latitude with a proper ARC.

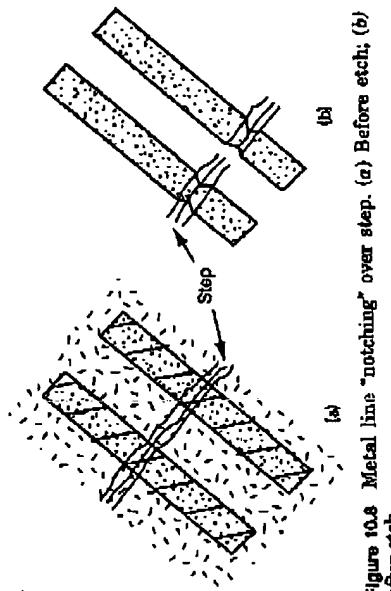


Figure 10.8 Metal line "notching" over step. (a) Before etch; (b) after etch.

An ARC is spun onto the wafer and baked. After the resist is spun on top of the ARC, the wafer is aligned and exposed. The pattern is developed in both the resist and the ARC. During the etch, the ARC acts as an etch barrier. To be effective, an ARC material must transmit light in the same range as the resist. It must also have good adhesion properties with the wafer surface and the resist. Two other requirements are that the ARC must have a refractive index that matches the resist, and that the ARC must develop and be stripped with the same chemicals as the resist.

There are several penalties associated with the use of an ARC. One is an additional layer requiring a separate spin and bake. The resolution gains offered by an ARC can be offset with poor thickness control and/or with an ill-controlled developing step. The time of exposure can increase 30 to 50 percent, increasing the wafer throughput time. ARC layers may also be used as the intermediate layer in a trilayer resist process or used on the top of the photoresist, called a top antireflective coating or TAR.

### Standing waves

In "Subsurface reflectivity," it was mentioned that the ideal exposure situation is when the radiation waves are directed to the wafer surface at 90°. This is true when only reflection problems are under consideration. However, 90° reflection causes another problem in positive photoresists, the creation of standing waves. As the radiation wave reflects off the surface and travels back up through the resist, it interferes constructively and destructively with the incoming wave, creating regions of varying energy (Fig. 10.10). The result after development is a rippled sidewall and a loss of resolution. A number of solutions are used to moderate standing waves, including dyes in the resist and separate

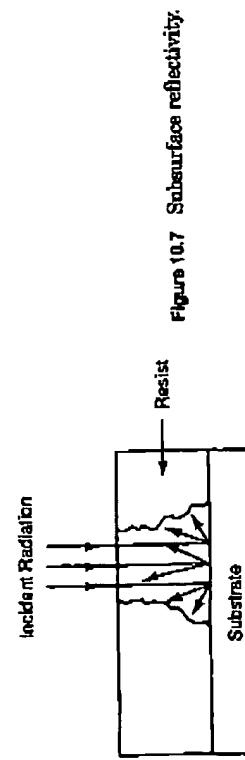


Figure 10.7 Subsurface reflectivity.